

Compal Confidential

ZAUSA Schematics Document

AMD "Kabini" Platform

AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun Pro S3

LA-A331P REV: 0.1

2013-02-04

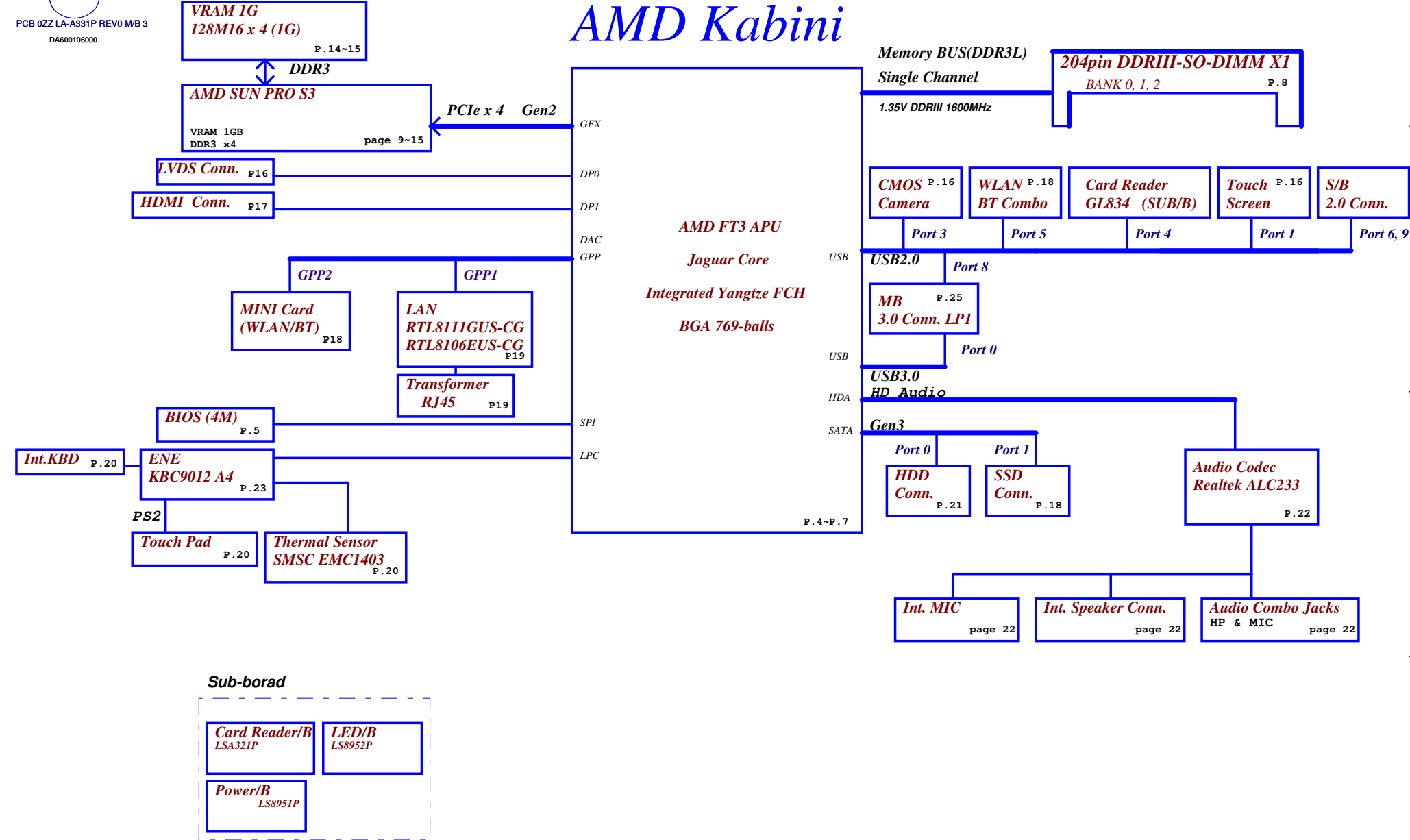
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Model Name : ZAUSA



AMD Kabini



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+0.95VALW	0.95V always on power rail	ON	ON	ON
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	PX	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	PX	OFF	OFF
+3VS_VGA	3.3V switched power rail for VGA	PX	OFF	OFF
+1.8VS_VGA	1.8V switched power rail for VGA	PX	OFF	OFF
+1.5VS_VGA	1.5V switched power rail for VGA	PX	OFF	OFF
+0.95VS_VGA	0.95V switched power rail for VGA	PX	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1 +3VALW	KB9012	X	V	X	X	X	X	X	X	X
APU_SCLK0 APU_SDAT0 +3VS	APU	X	X	X	V	V	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2 +3VS	KB9012	V	X	X	X	X	V	X	V	X

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

APU
SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	EVT
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
		0	RIGHT USB
		1	Touch Screen
		2	
		3	Camera
		4	CardReader
		5	WLAN/BT Combo
		6	LEFT USB2.0
		7	
	XHCI	0	LEFT USB3.0
		1	LEFT USB2.0

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

USB OC MAPPING

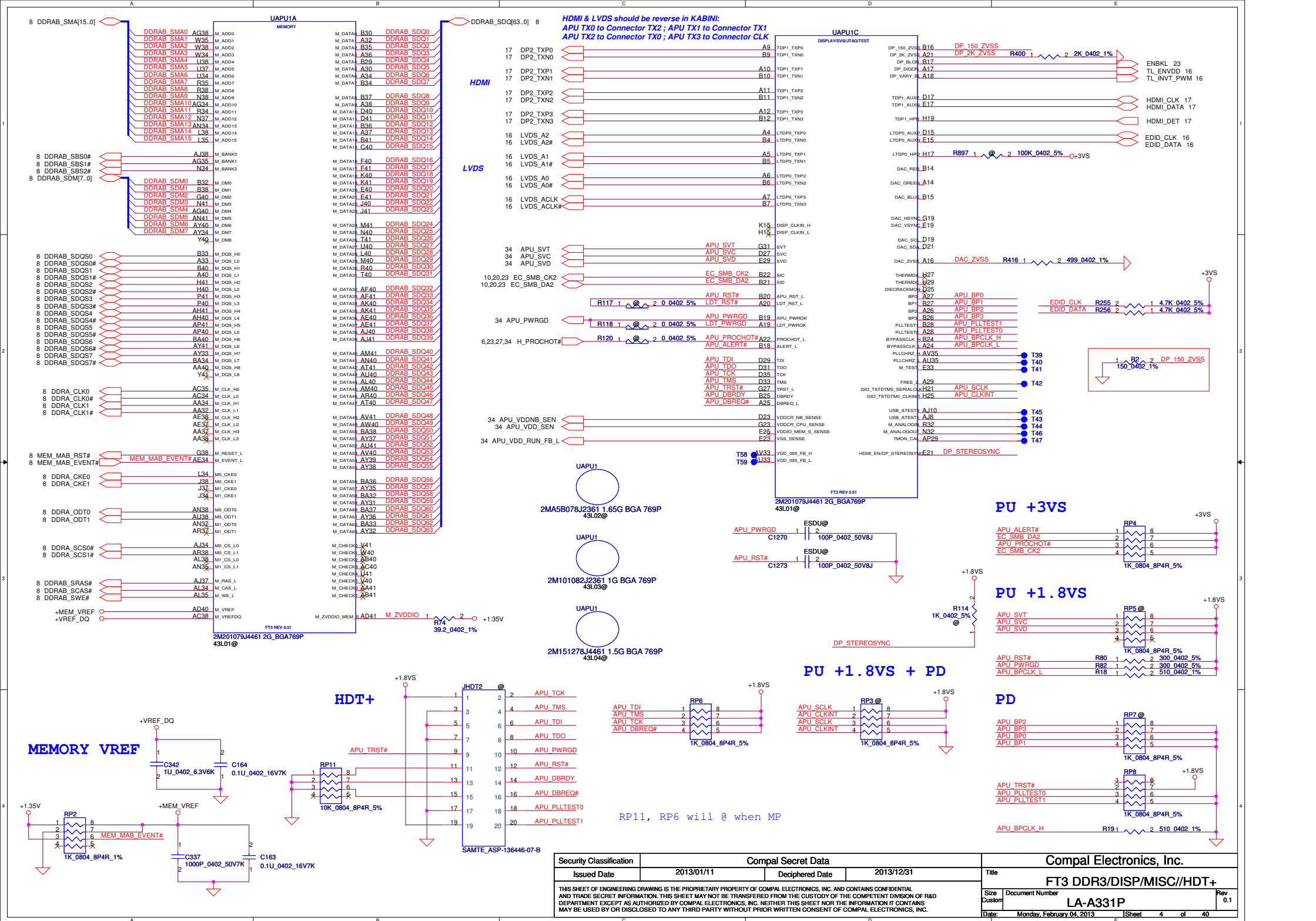
OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

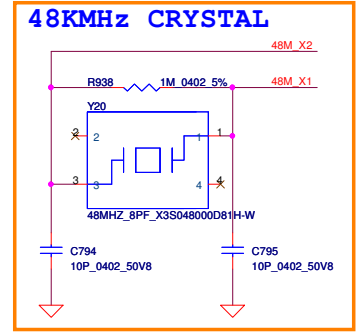
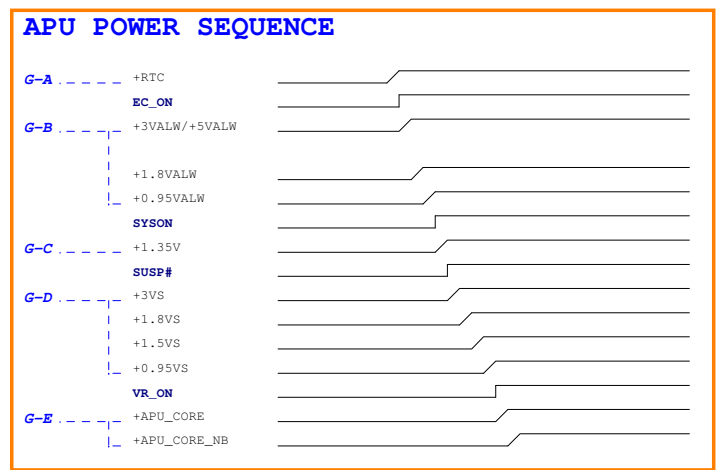
43190S38L01: EMIP@/ESDP@/SWR@/8106@/TS@/UMA@/43L01@
43190S38L02: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L02@
43190S38L03: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L03@
43190S38L04: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L04@

BOM Structure Table

BOM Structure	BTO Item
43L01@	X4-5110 BGA APU
43L02@	X2-3450 BGA APU
43L03@	E1-2210 BGA APU
43L04@	X4-4110 BGA APU
ME@	ME part
SWR@	LAN Switching mode
LDO@	LAN LDO mode
GAS@	Gastube
PX@	Common VGA circuit
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
X76@	VRAM
VRAM1@	Samsung 128Mbx16 K4W2G1646E-BC1A
VRAM2@	Hynix 128Mbx16 H5TC2G63FFR-11C
VRAM3@	Micron 126Mbx16 MT41J128M16JT-093G:K
8111@	Realtek RTL8111GUS-CG (Giga LAN)
8106@	Realtek RTL8106EUS-CG (10/100M)
@	Unpop

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Size Custom		Document Number		Rev 0.1	
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4MB SPI ROM
(Current Share mode)

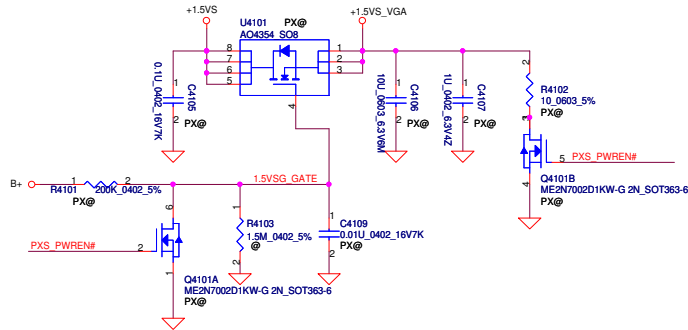
APU->EC->ROM must route as
Daisy Chain for Share ROM quality

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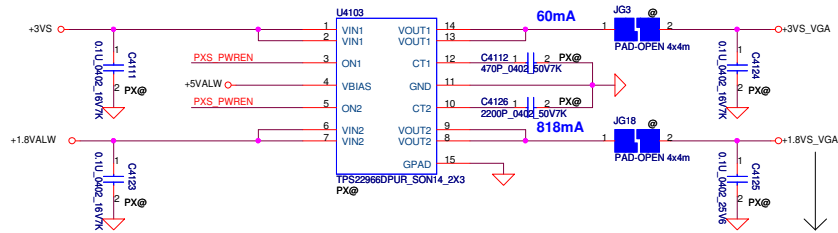


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+1.5VS to +1.5VS_VGA (2.096A)



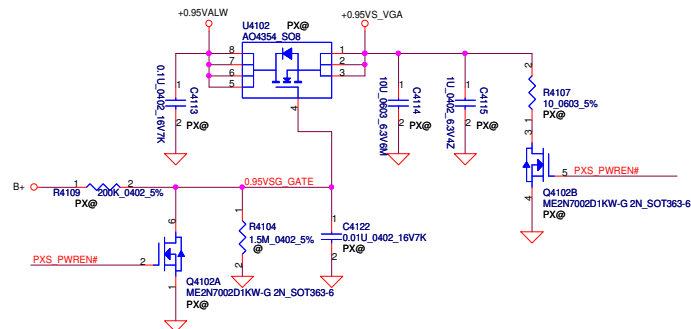
+3VS to +3VS_VGA (25mA) +1.8VALW to +1.8VS_VGA (311mA)



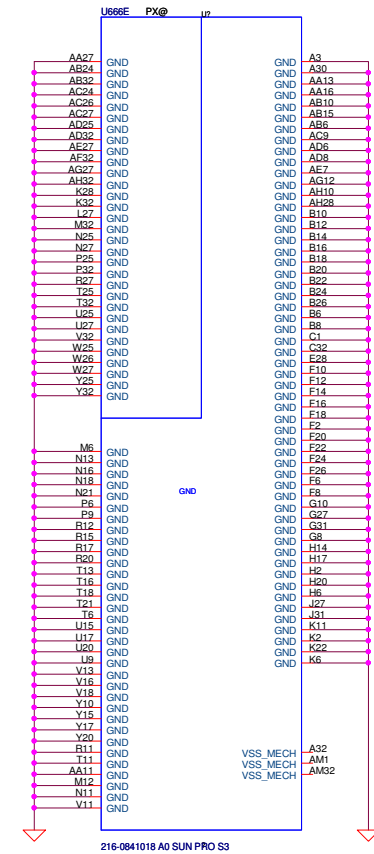
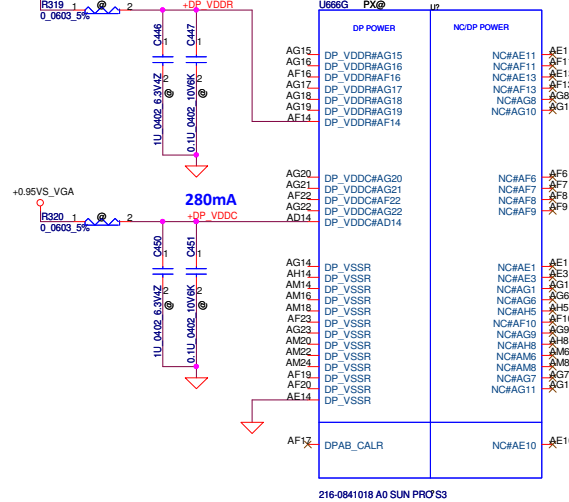
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, A021331 (engineering sample available on 2013/Jan/18)

+1.8VS_VGA 必须比 +VGA_CORE晚起来

+0.95VALW to +0.95VSG (4.016A)



370mA (HDMI) 188mA (Display Port) No Use GPU Display Port output



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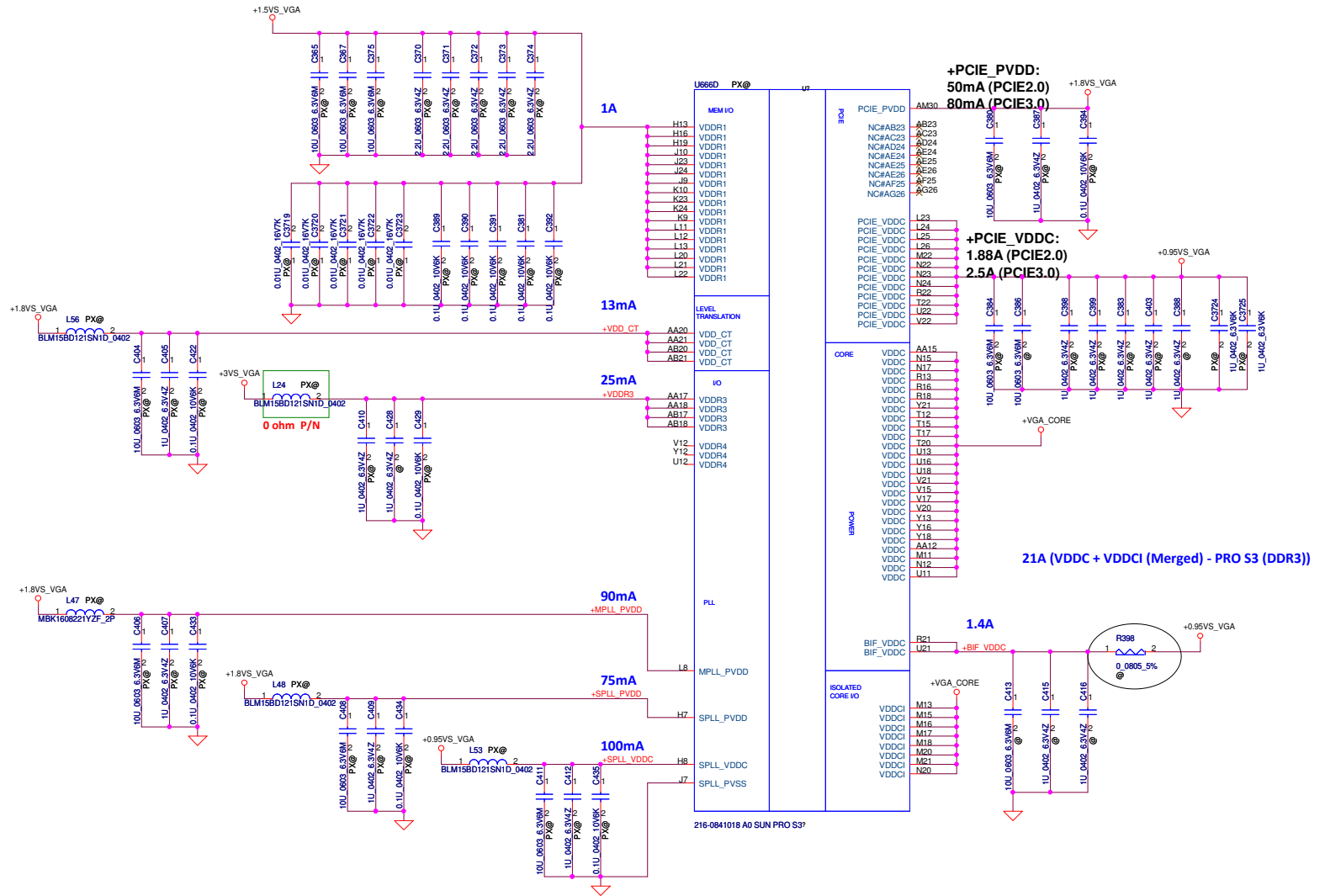
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

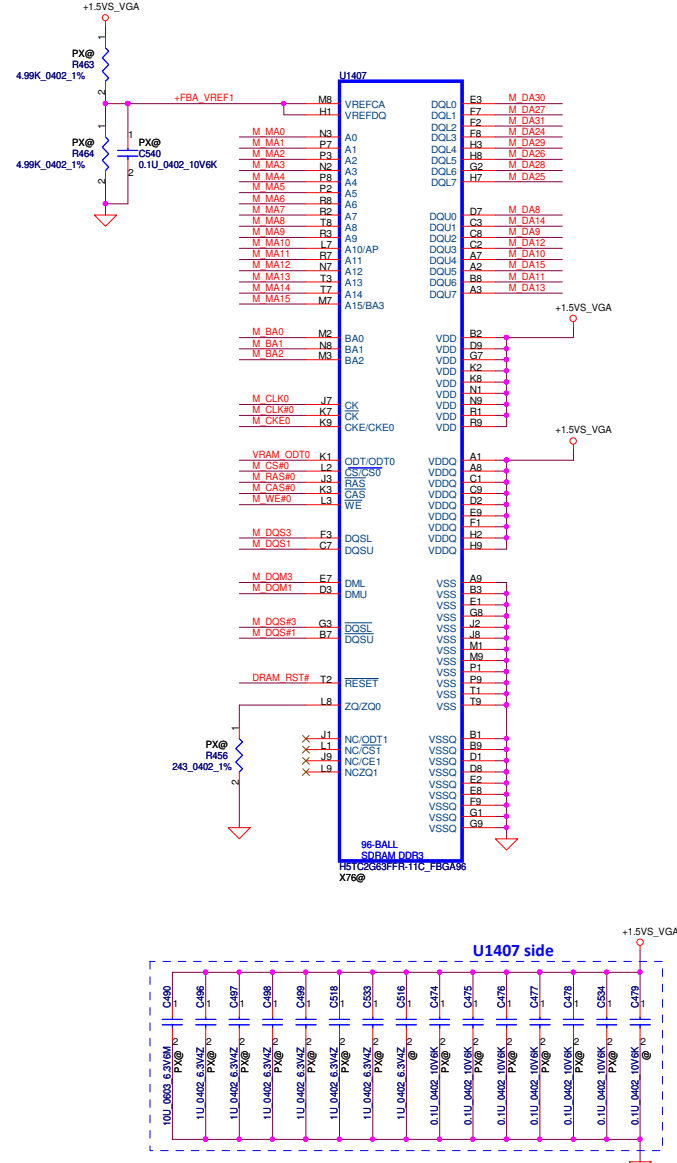
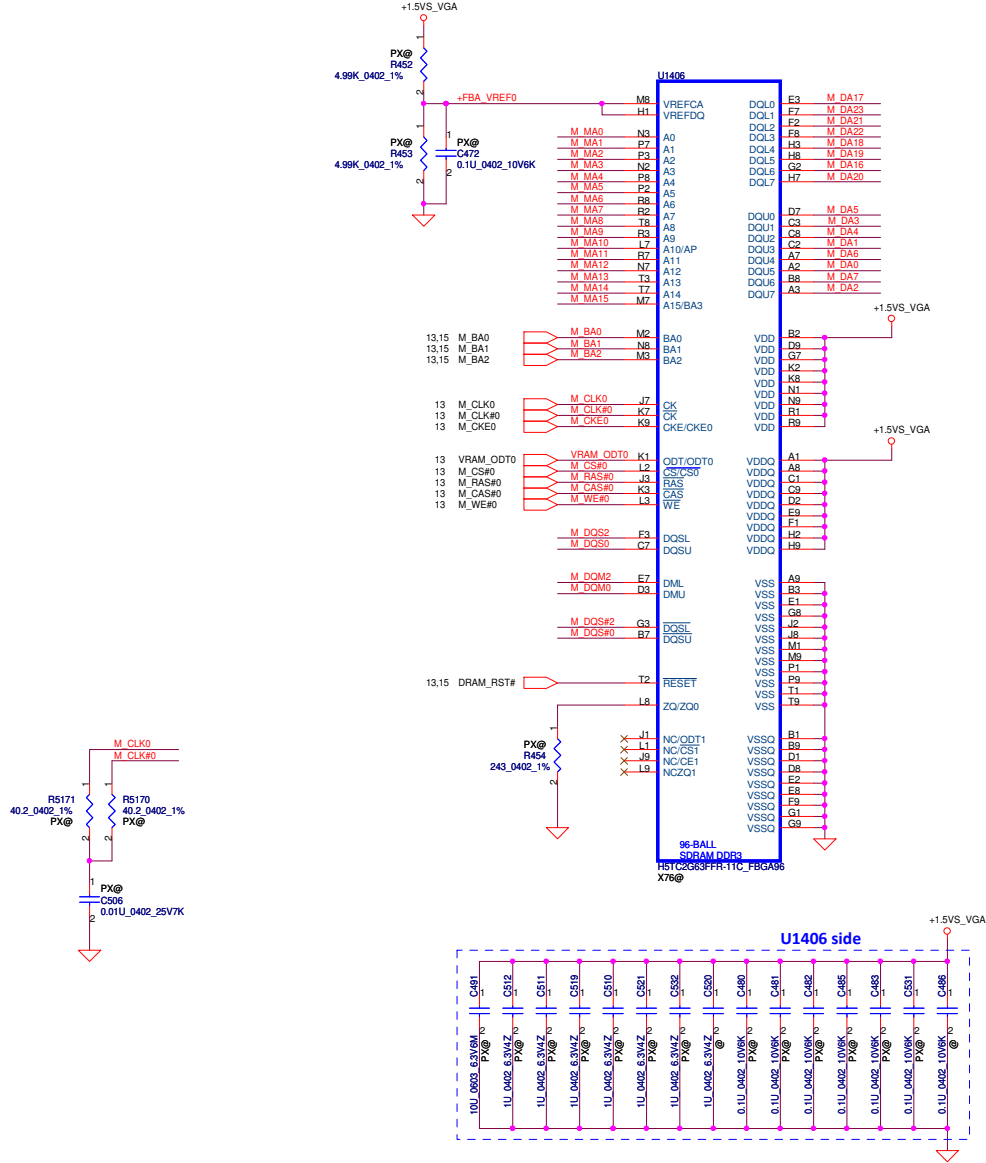
+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)

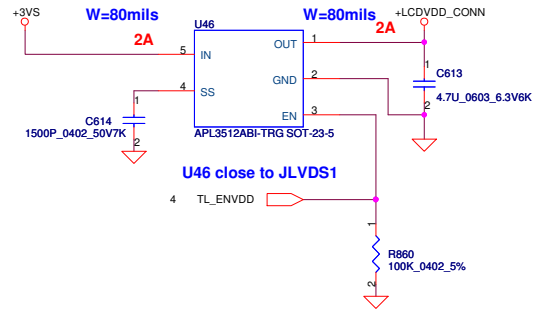


Memory Partition A - Lower 32 bits

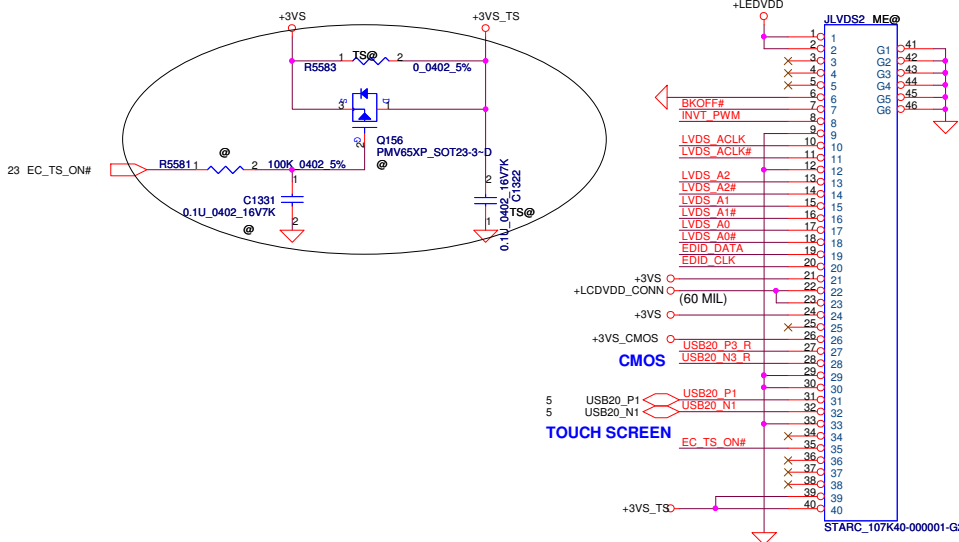
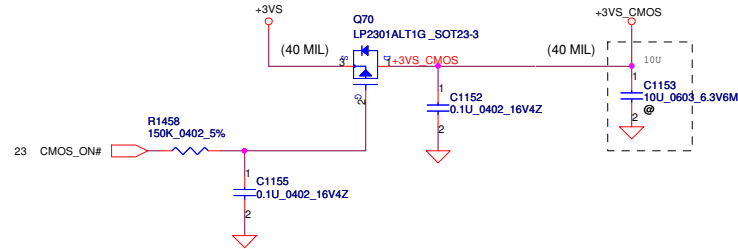
- 13,15 M_DA[63..0] M_DA[63..0]
- 13,15 M_MA[15..0] M_MA[15..0]
- 13,15 M_DQM[7..0] M_DQM[7..0]
- 13,15 M_DQS[7..0] M_DQS[7..0]
- 13,15 M_DQS#[7..0] M_DQS#[7..0]



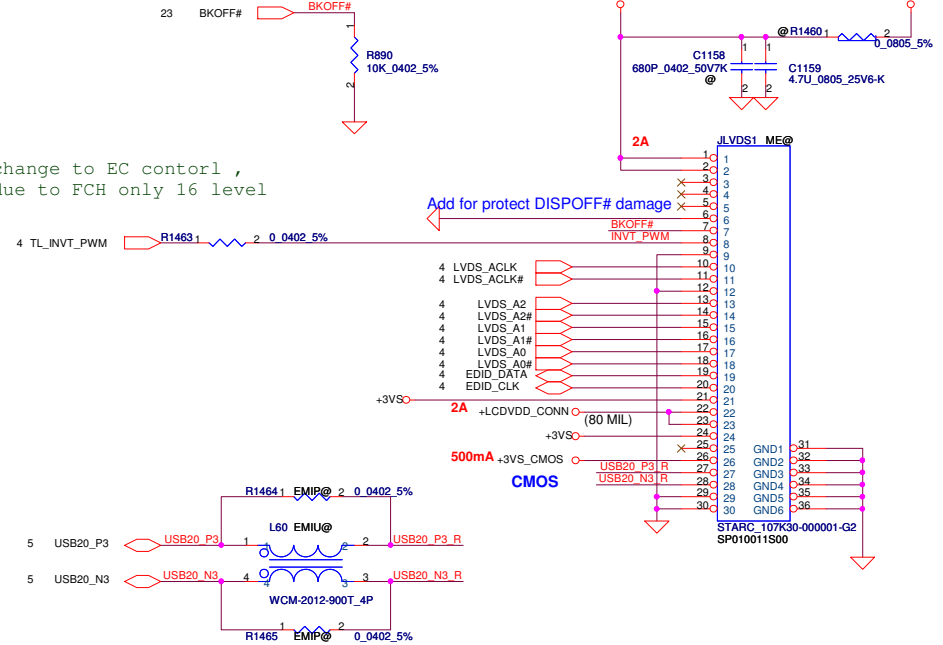
LCD POWER CIRCUIT



CMOS Camera



change to EC control ,
due to FCH only 16 level



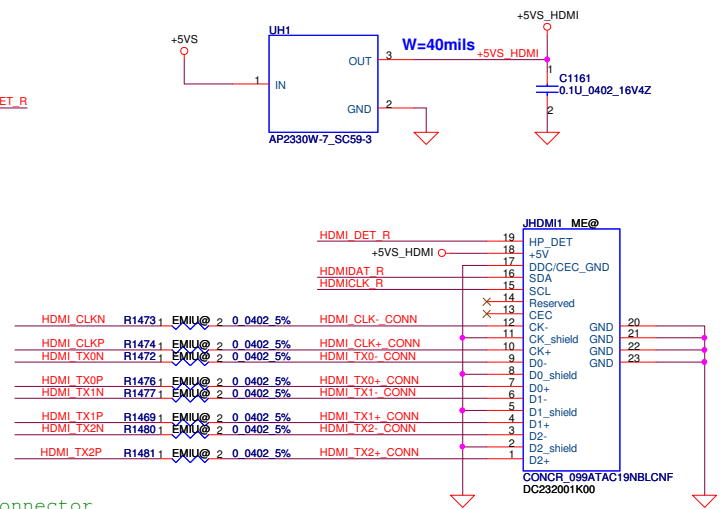
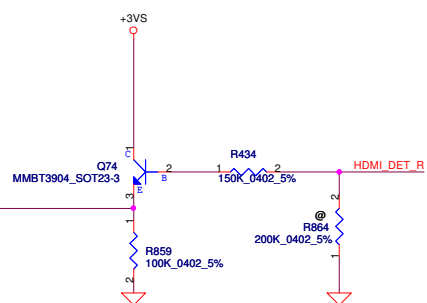
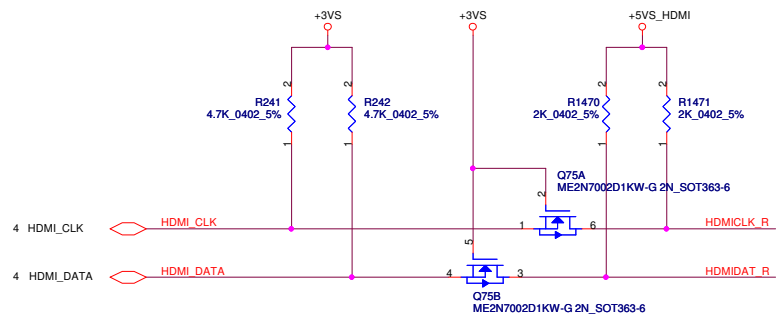
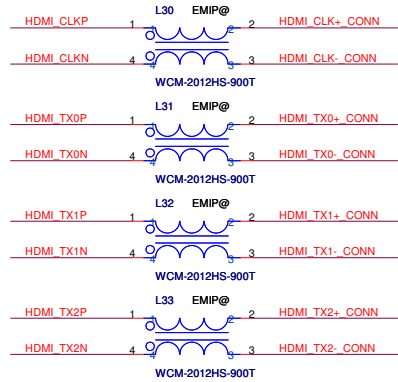
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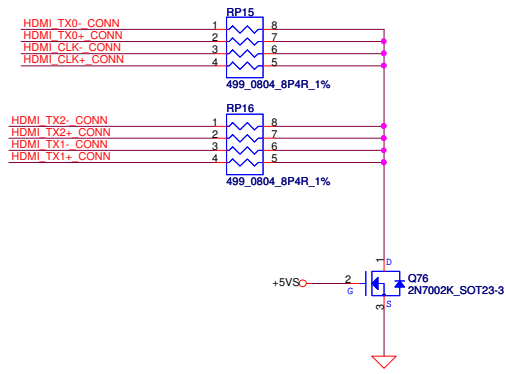
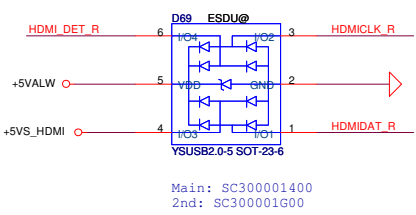
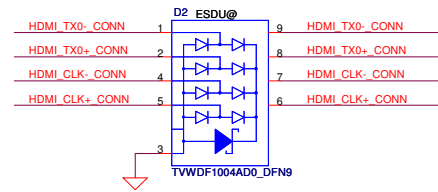
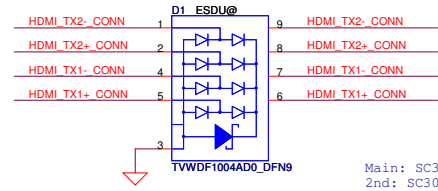
LVDS/CAMERA

Rev 0.1

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4	DP2_TXN0	DP2_TXN0	C47	1	2	0.1U_0402_16V7K	HDMI_TX2N
4	DP2_TXP1	DP2_TXP1	C48	1	2	0.1U_0402_16V7K	HDMI_TX1P
4	DP2_TXN1	DP2_TXN1	C55	1	2	0.1U_0402_16V7K	HDMI_TX1N
4	DP2_TXP2	DP2_TXP2	C56	1	2	0.1U_0402_16V7K	HDMI_TX0P
4	DP2_TXN2	DP2_TXN2	C68	1	2	0.1U_0402_16V7K	HDMI_TX0N
4	DP2_TXP3	DP2_TXP3	C72	1	2	0.1U_0402_16V7K	HDMI_CLKP
4	DP2_TXN3	DP2_TXN3	C74	1	2	0.1U_0402_16V7K	HDMI_CLKN

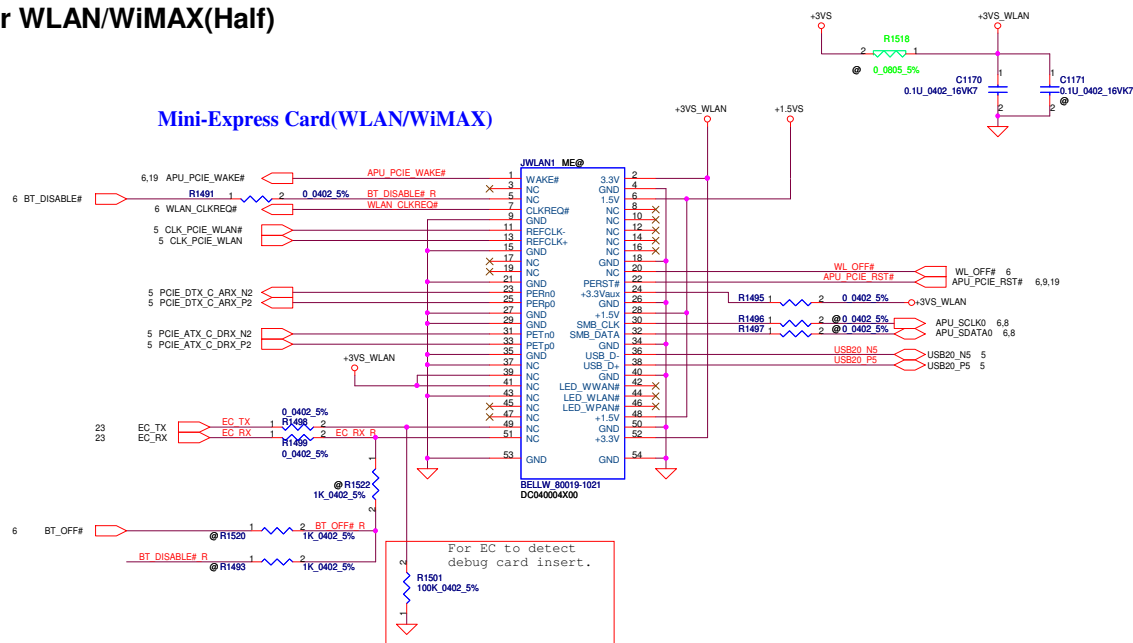


Close to HDMI connector

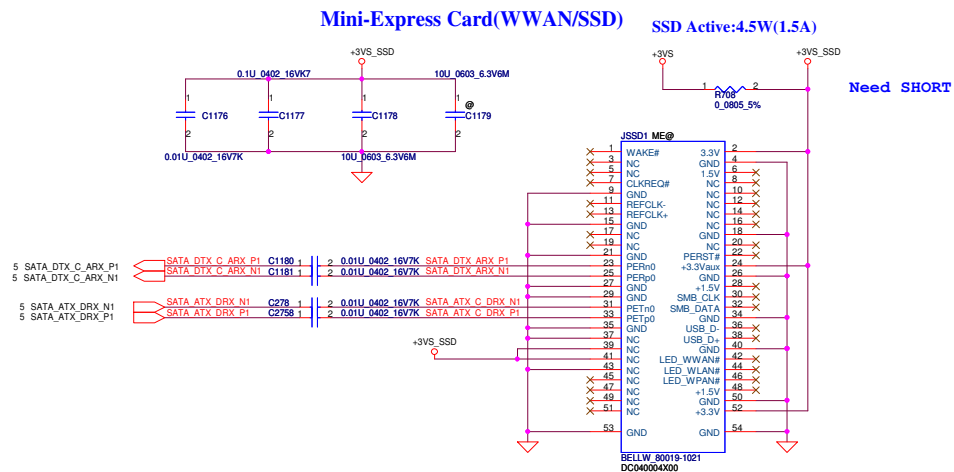


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Mini-Express Card for WLAN/WiMAX(Half)



Mini-Express Card for SSD(Full)

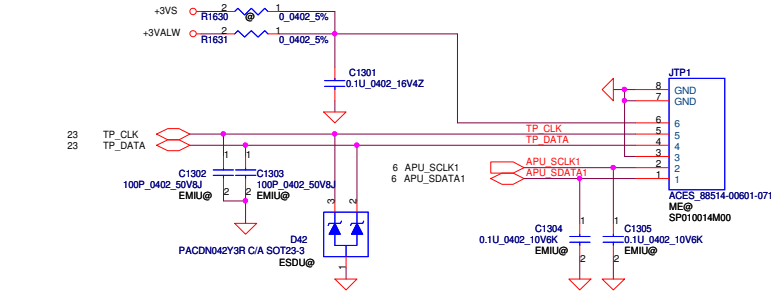


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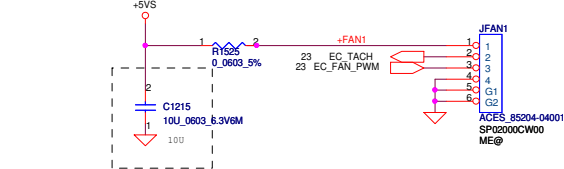
INT_KBD Conn.



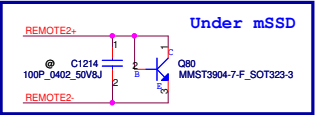
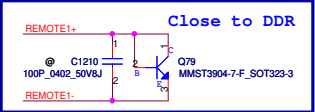
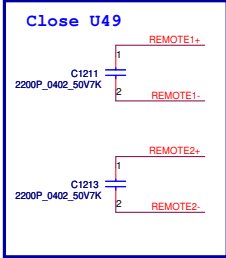
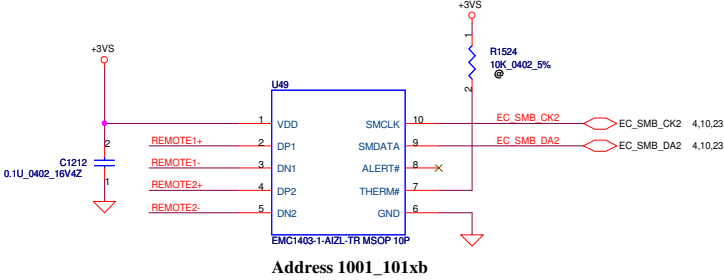
Touch PAD Module



FAN1 Conn

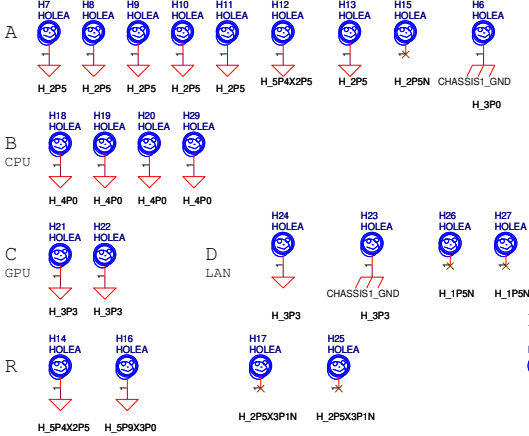


SMSC thermal sensor placed near by VRAM



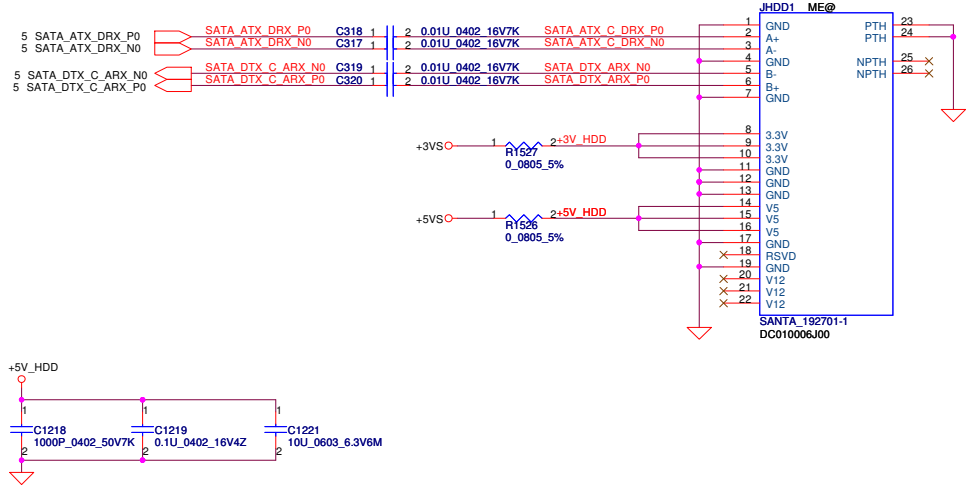
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Screw Hole



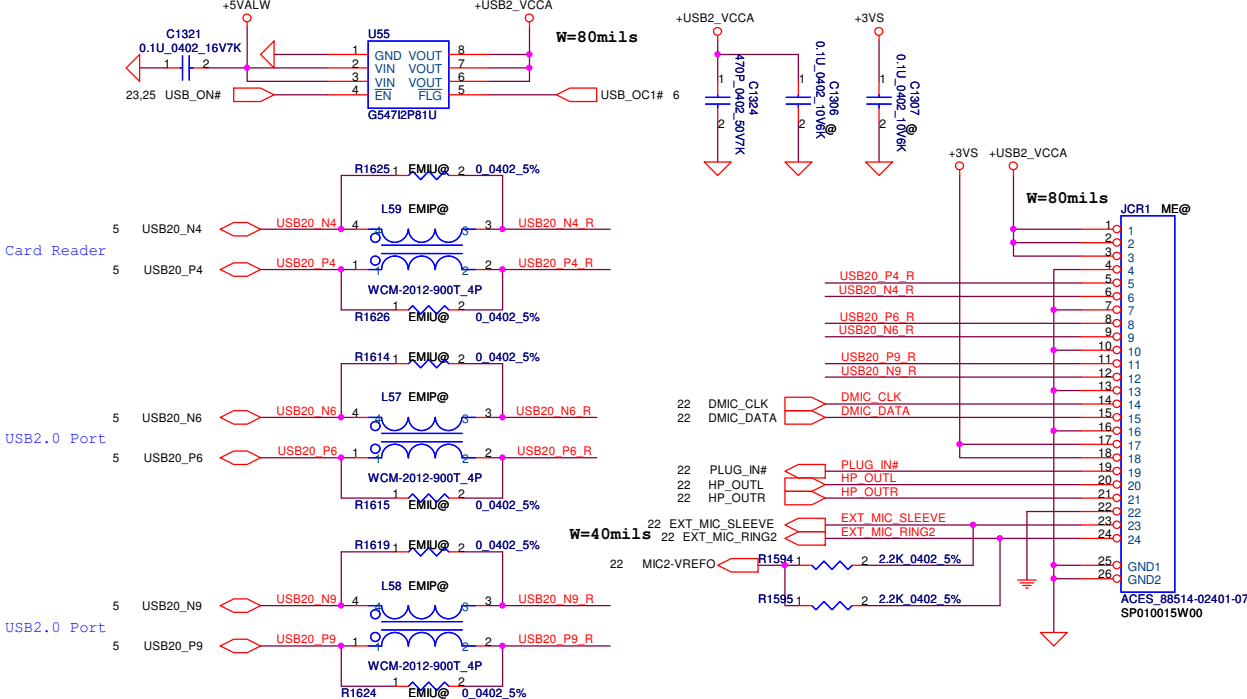
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	
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Size		Document Number		Rev	
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Date: Monday, February 04, 2013		Sheet		20 of 40	

SATA HDD Conn.

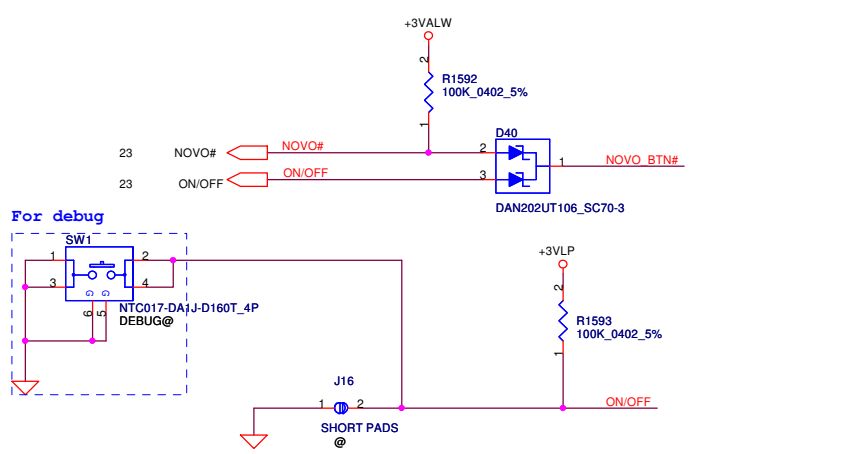
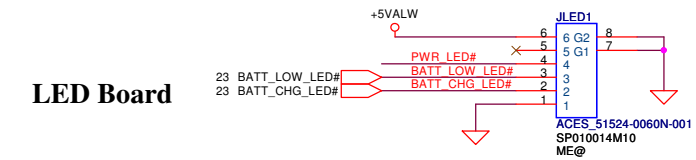


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				Date	Monday, February 04, 2013
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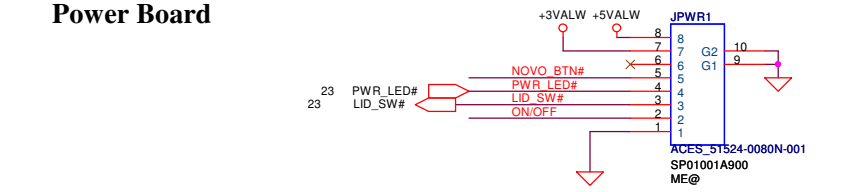
IO Board



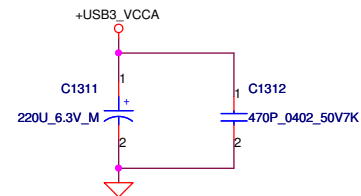
LED Board



Power Board



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W=80mils

LP1

JUSB1

9 1 8 7 6 5 4 3 2 1

USB30 TX R P0

USB30 TX R N0

USB30 P8 R

USB30 N8 R

USB30 RX R P0

USB30 RX R N0

GND

D-

D+

10 11 12 13

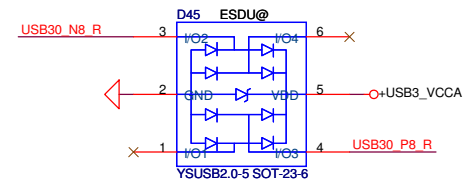
GND

GND

GND

TAITW_PUBAU1-09FNLSCNN4H0

ME@



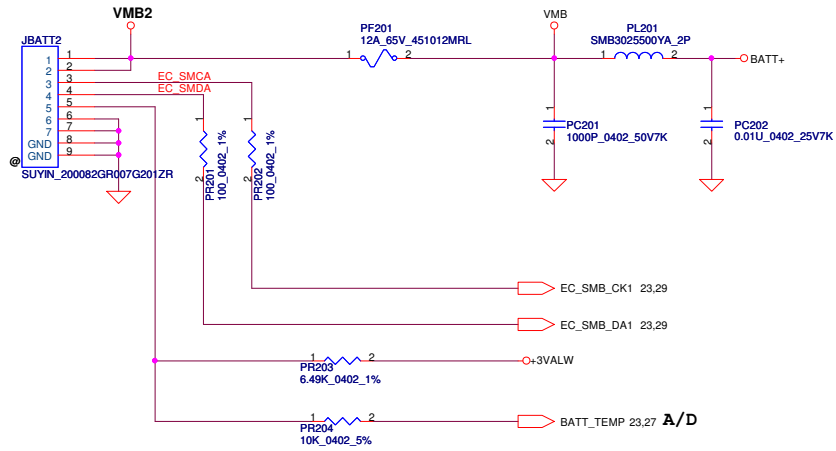
The diagram illustrates the internal circuitry of the USB to RS485 module. The USB-D44 connector is shown with the following connections:

- Pin 1:** USB30 RX_R_P0
- Pin 2:** USB30 RX_R_P0
- Pin 3:** USB30 TX_R_P0
- Pin 4:** USB30 TX_R_P0
- Pin 5:** USB30 TX_R_P0
- Pin 6:** USB30 TX_R_P0
- Pin 7:** USB30 TX_R_P0
- Pin 8:** TVWDF1004AD0 DFN ESD

The circuit includes a TVWDF1004AD0 chip and an ESDU component. The USB signals are connected to the TVWDF1004AD0 chip via a network of resistors and diodes. The ESDU component is connected to the TVWDF1004AD0 chip and the ESD pin.

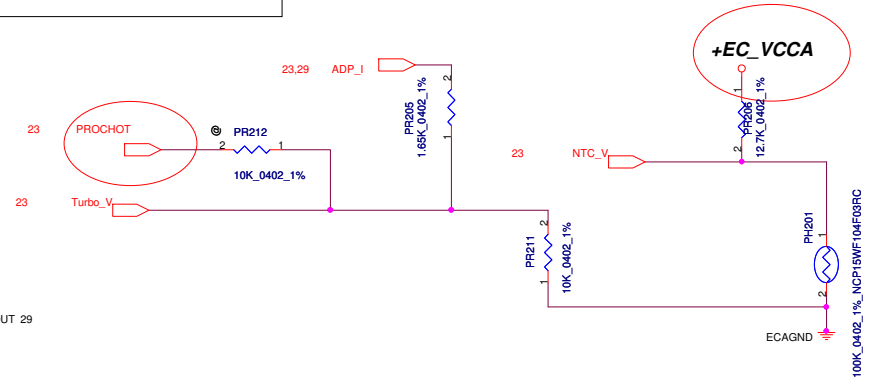
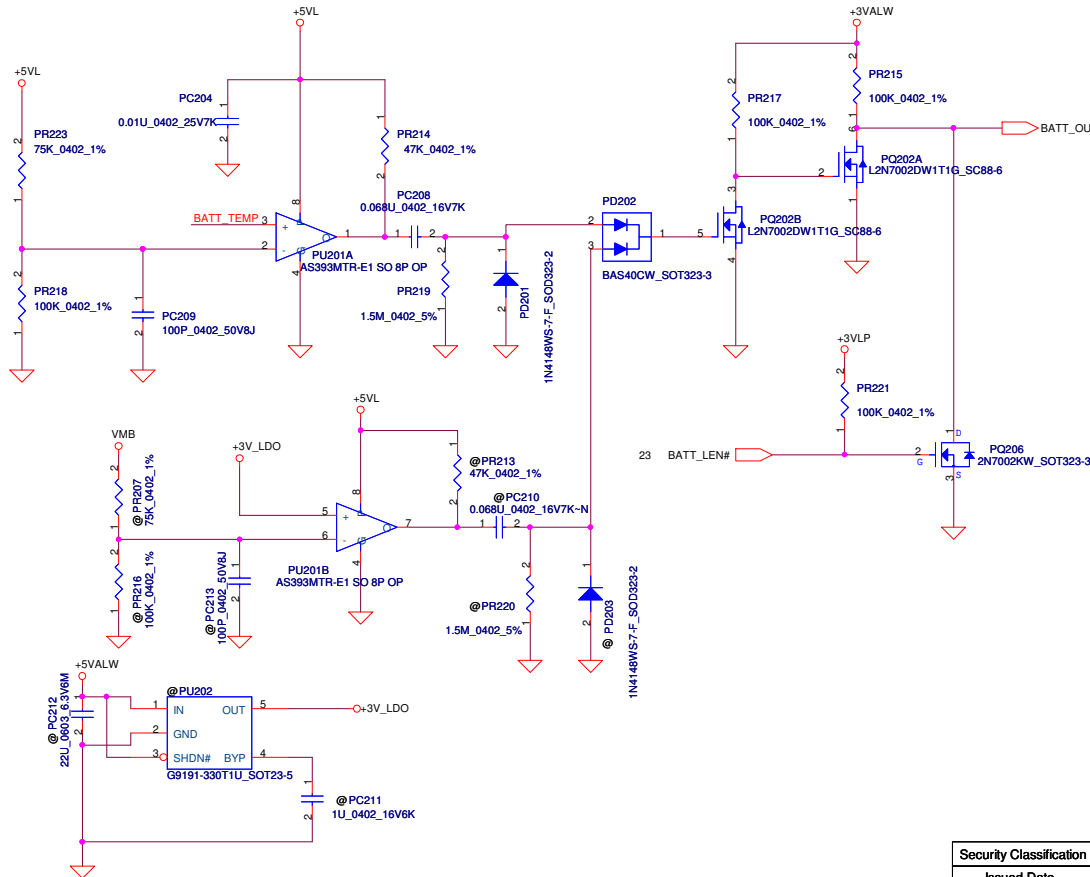
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JBATT2 Just for 14"

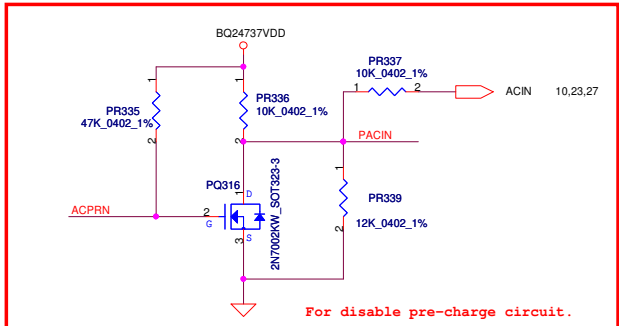


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

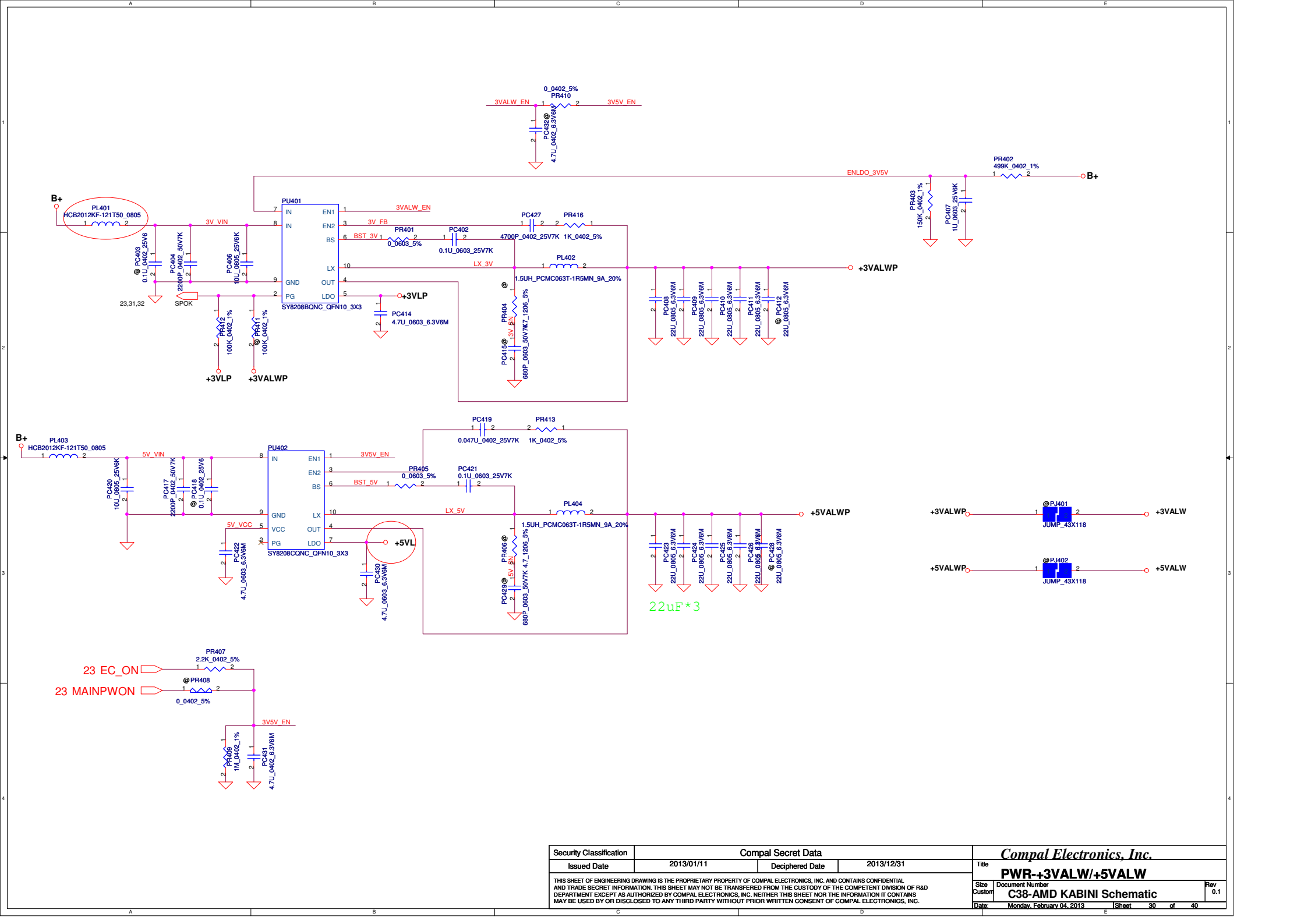
65W(UMA) : PR205=1.65K(SD034165180)



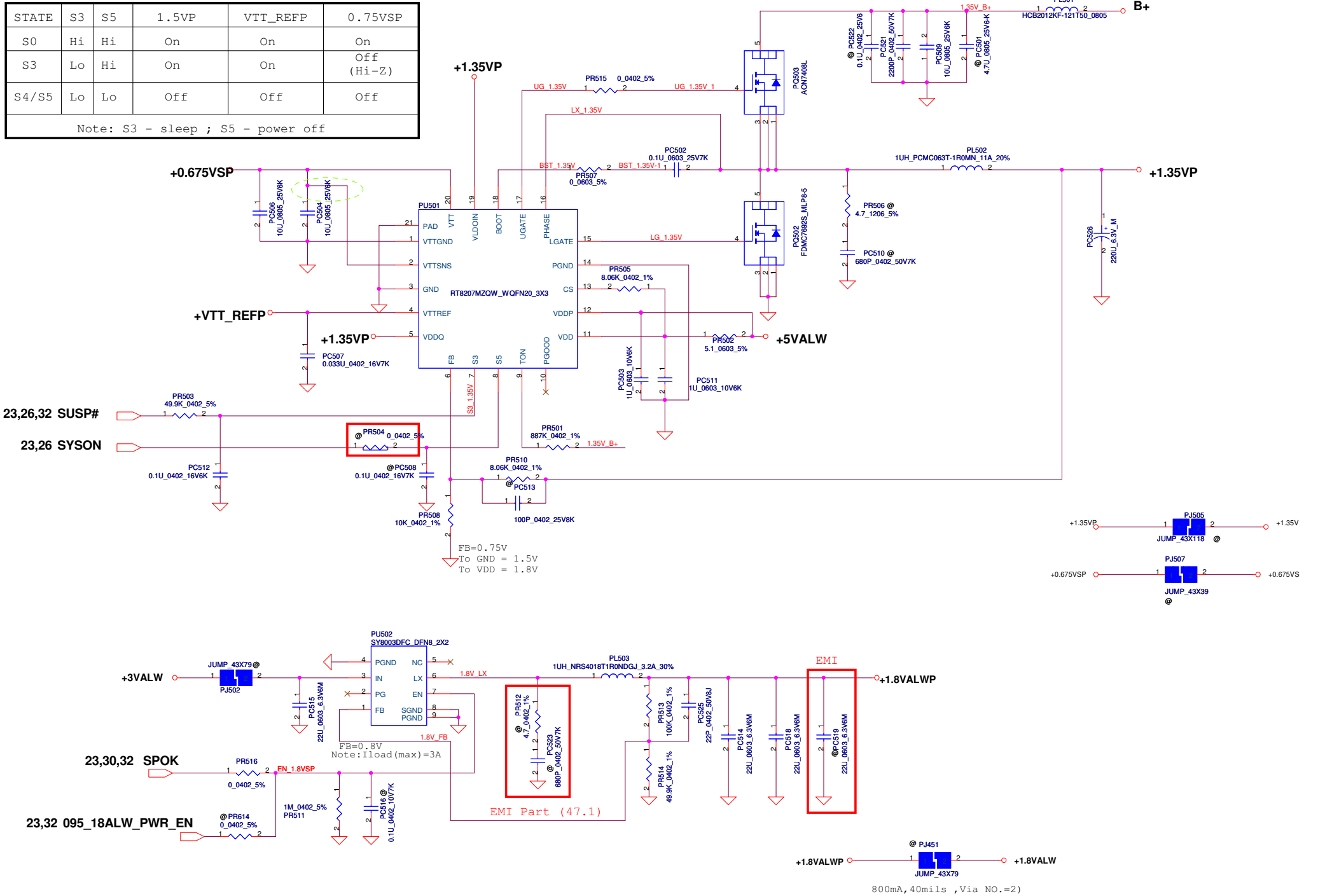
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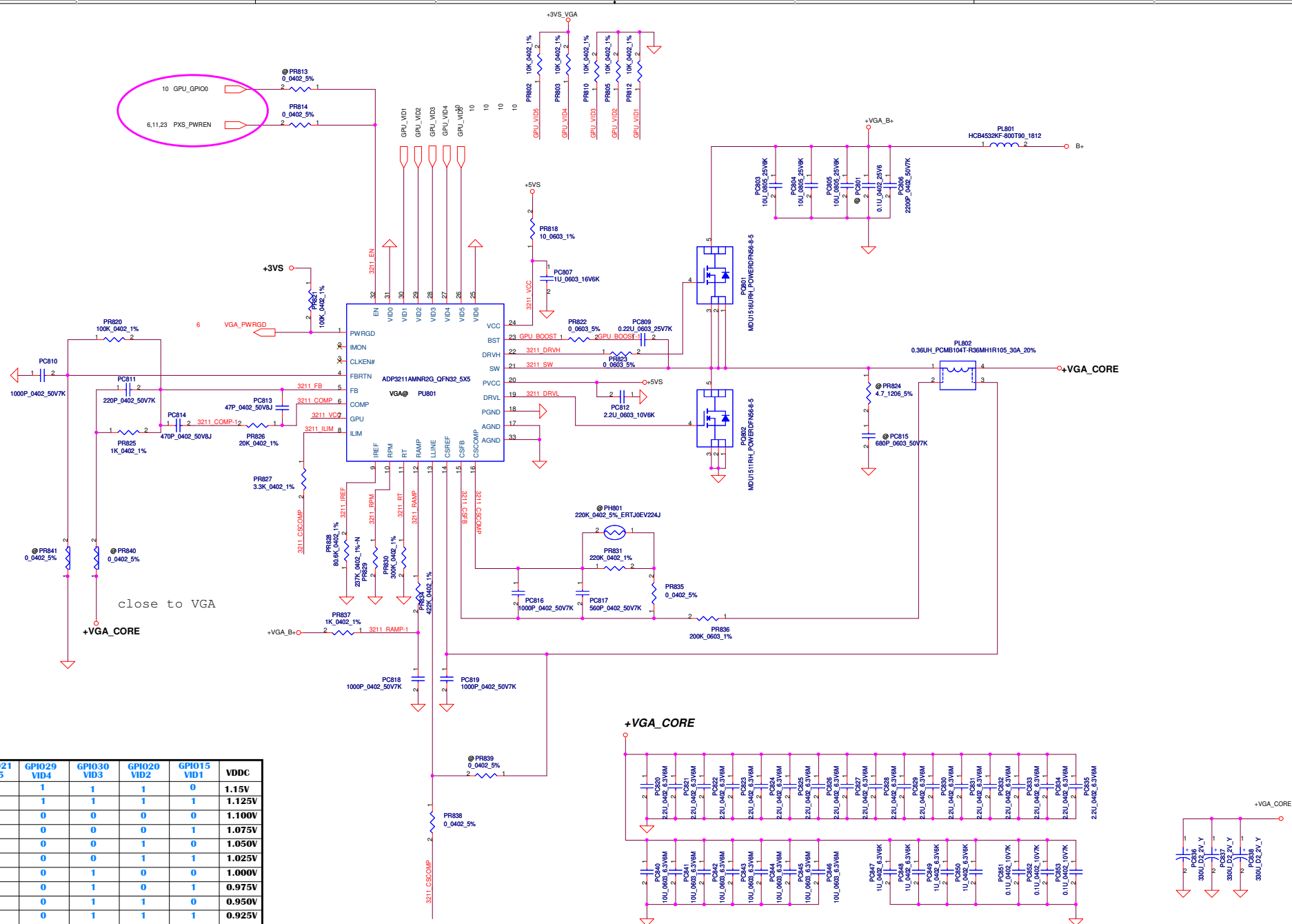


STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



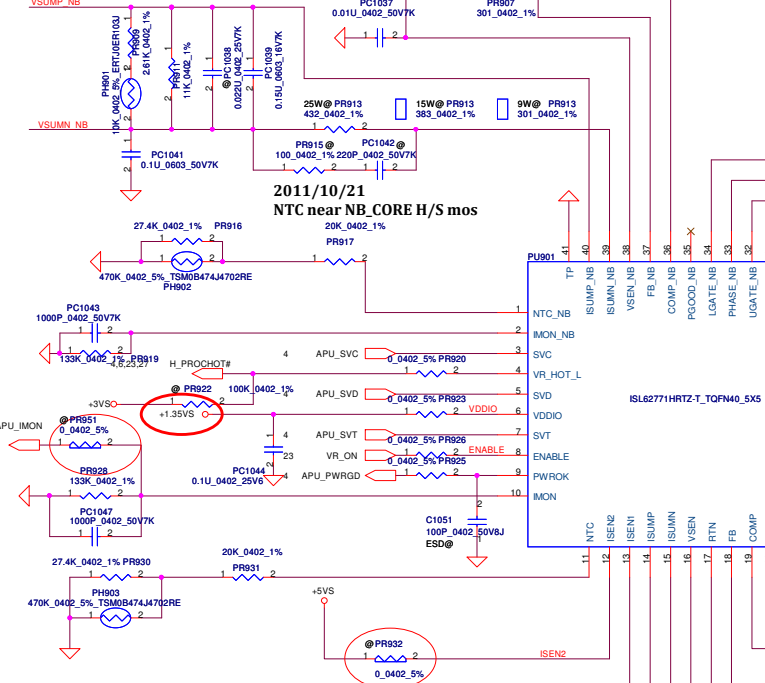
GPIO21 VID5	GPIO29 VID4	GPIO30 VID3	GPIO20 VID2	GPIO15 VID1	VDDC
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default



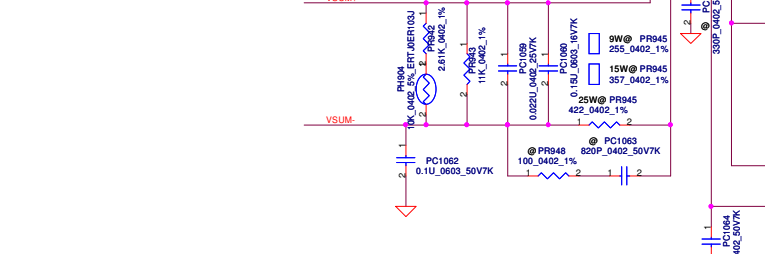
2011/10/21

NTC near phase 1 choke



2011/10/21

NTC near CPU_CORE H/S mos

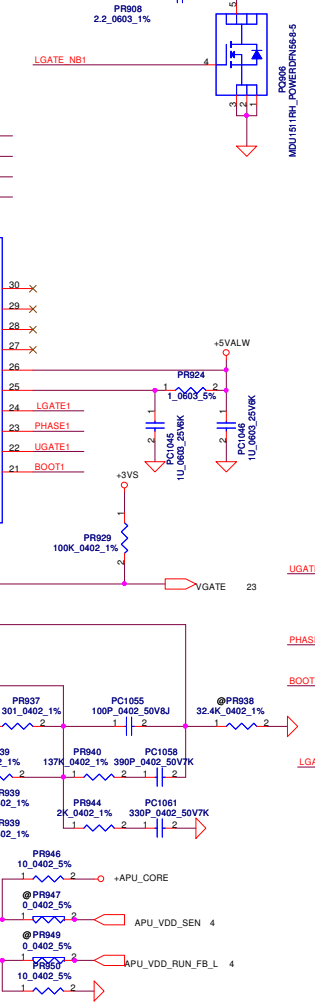


2011/10/21
NTC near phase 1 choke

2012/10/30

Load Line: VDD-->4m

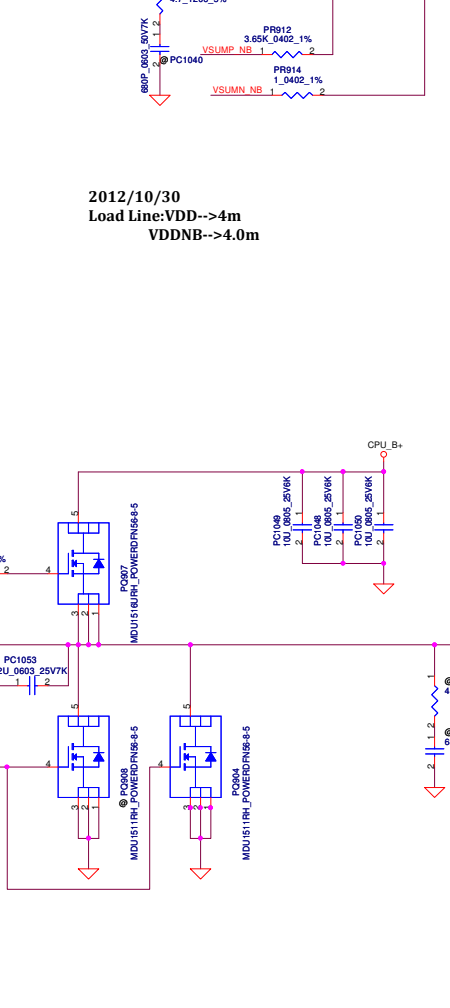
VDDNB-->4.0m



SH00000K00 (DCR 1.4+-5%)

PL901

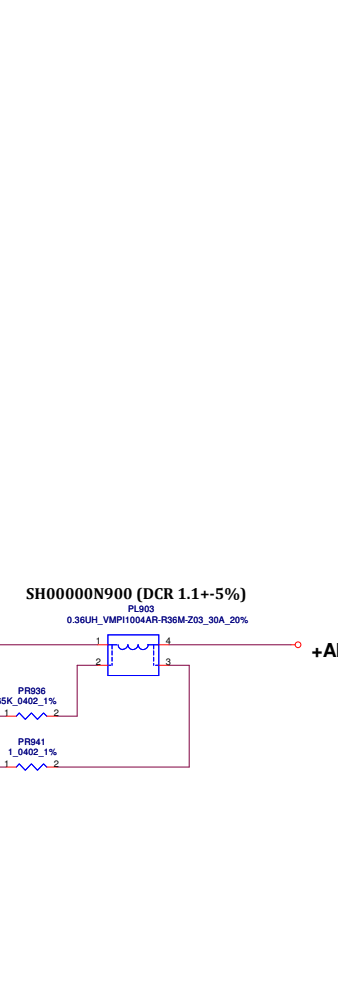
0.36UH_VMPH11004AR-R36M-20A_20%



SH00000N900 (DCR 1.1+-5%)

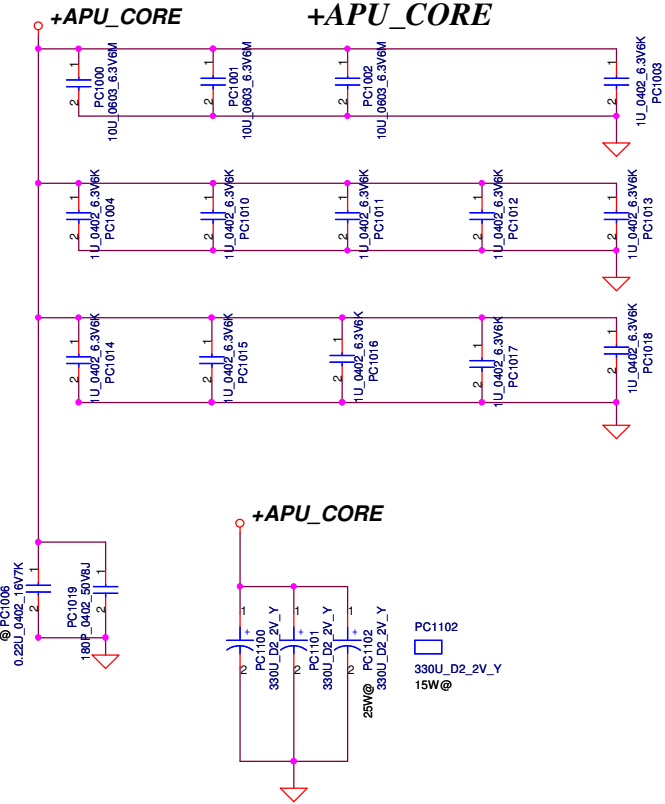
PL903

0.36UH_VMPH11004AR-R36M-20A_20%

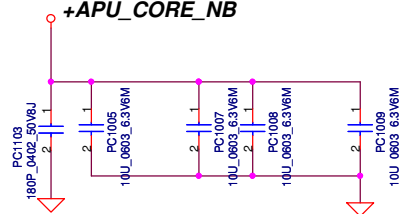


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										C38-AMD KABINI Schematic		0.1	
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CPU_Core output CAP (Including MLCC) 36.4

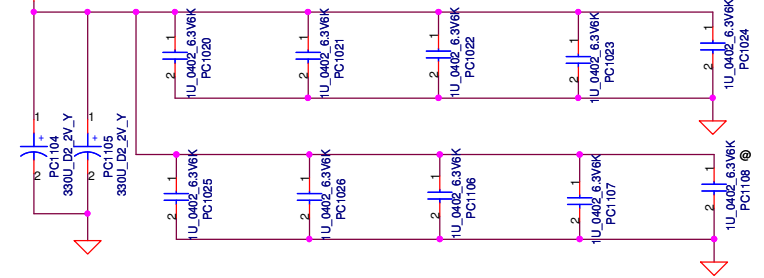


+APU_CORE_NB



GFX output CAP (Including MLCC) 36.5

Local +APU_CORE_NB



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				A3	C38-AMD KABINI Schematic	0.1
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Item	Modify List	PG#	Reason for change	Date	Phase
1					
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9					
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for HW*

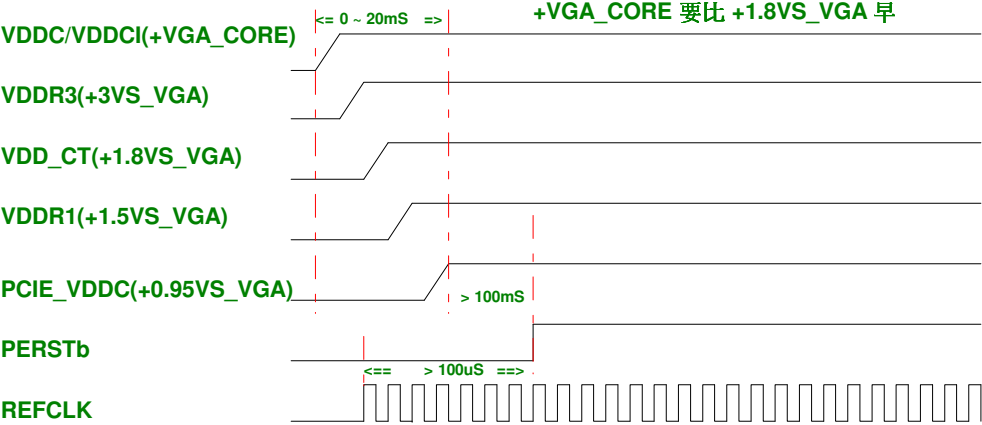
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				Size	Document Number	Rev
				Custom	C38-G series Chief River Schematic	0.1
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Power-Up/Down Sequence

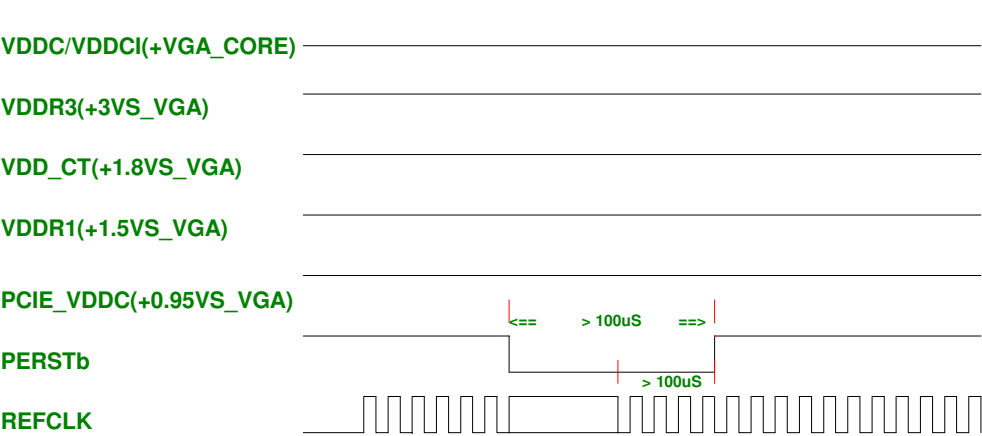
"Sun" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

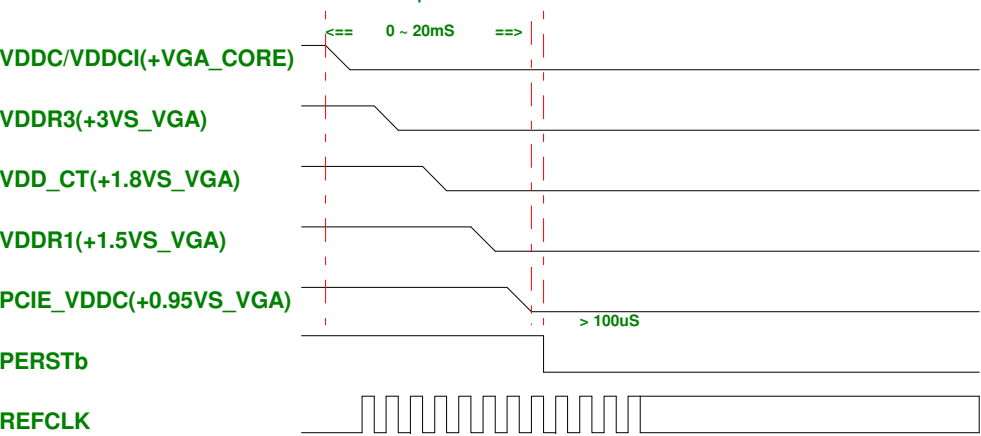
Cold Boot Sequence



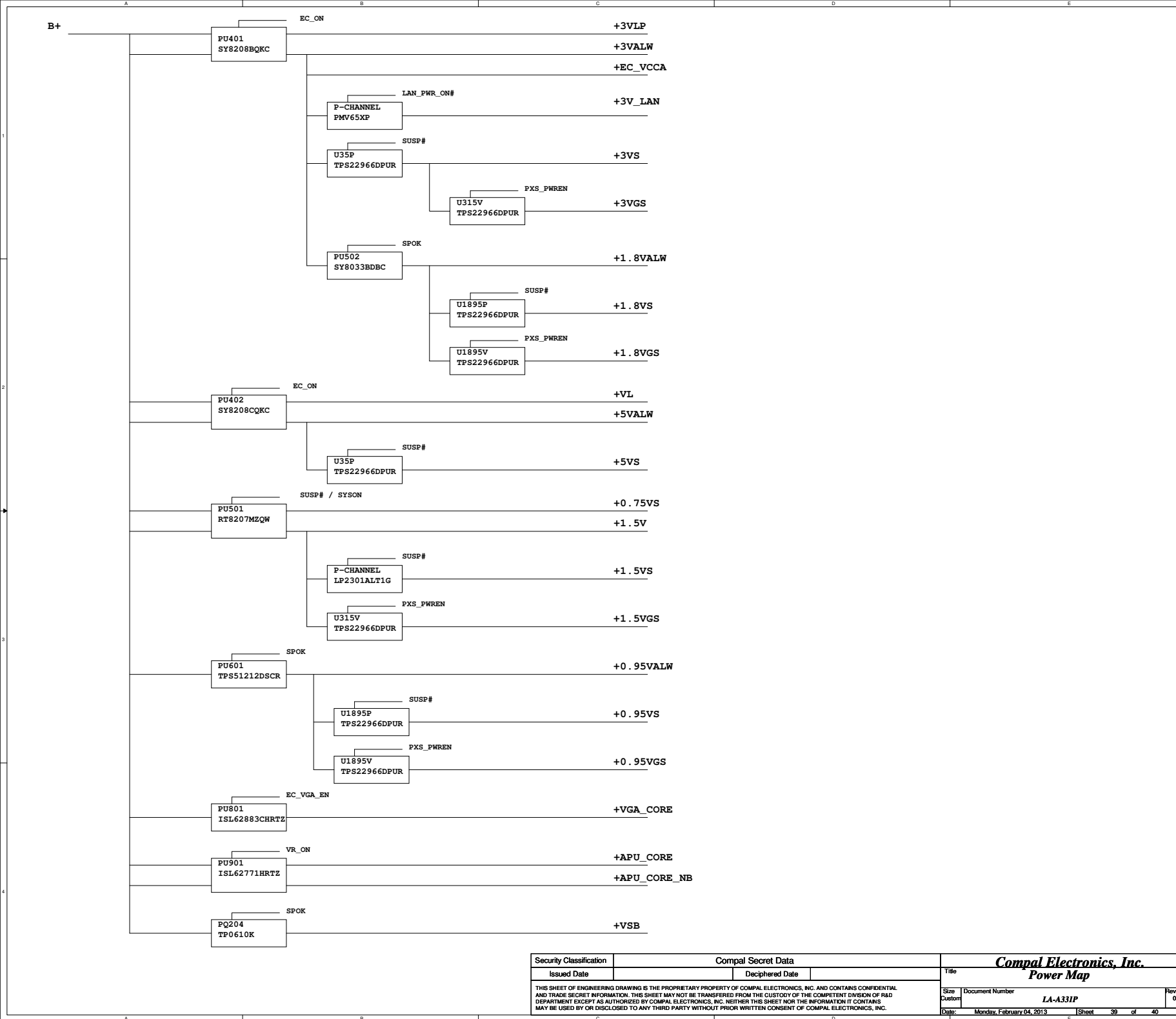
Warm Boot Sequence

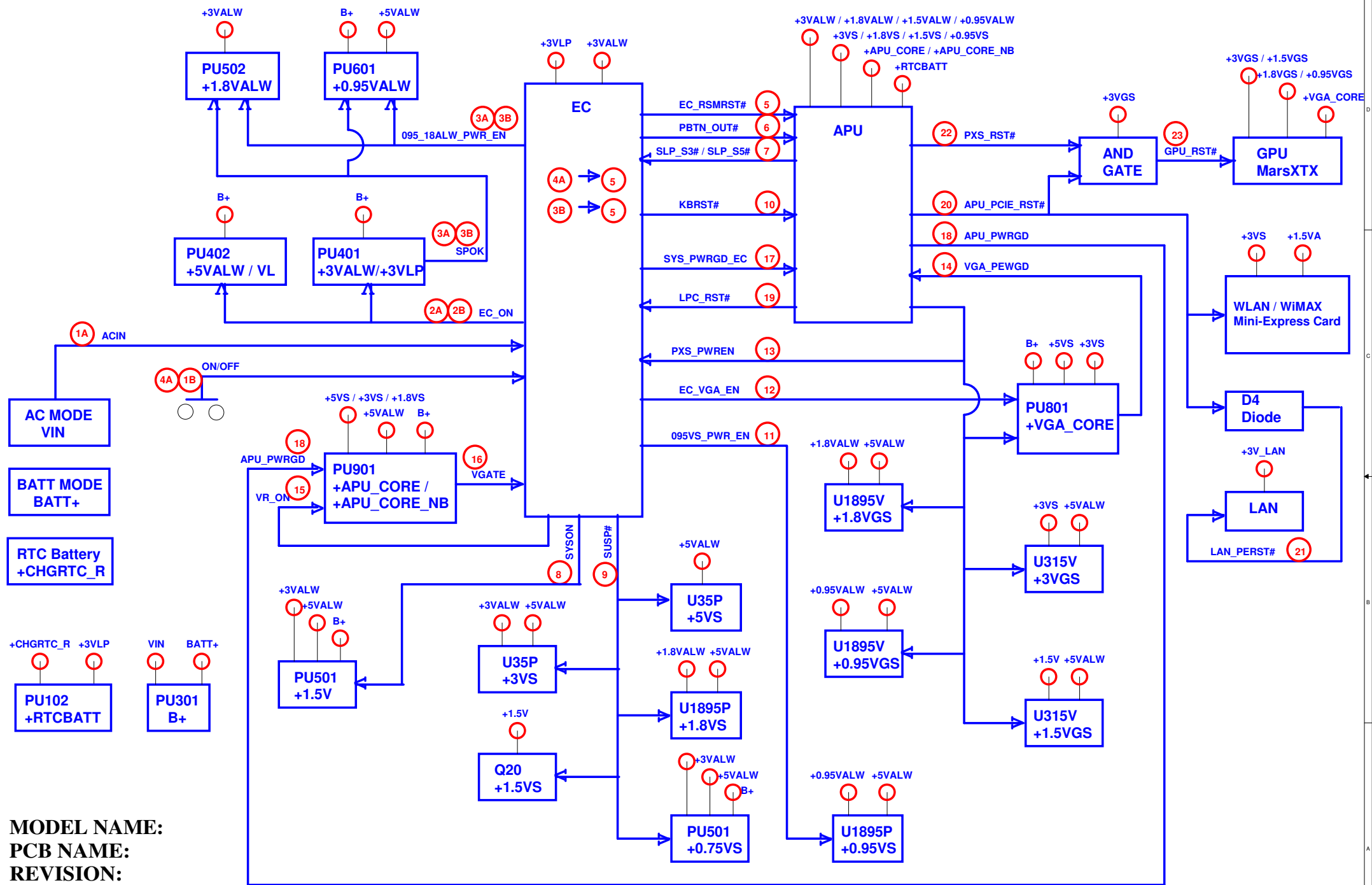


Power Down Sequence



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MODEL NAME:
PCB NAME:
REVISION:
DATE: 2011/11/23

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